X-band 768-channel system

Two-dimensional active phased array antenna

1.Product Composition and Technical Specifications

Product Information

The X-band 768-channel two-dimensional active phased array antenna consists of 768 antenna elements, comprising several components: the antenna 罩 (antenna cover), AIP module, sum-and-difference module, power supply waveform control module, frequency synthesizer module, cable assembly, and structural components.

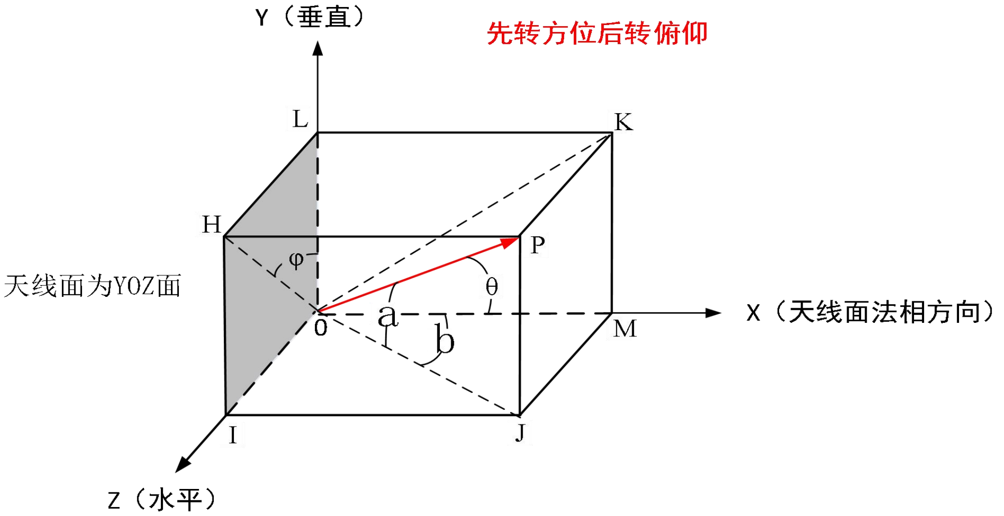
During reception, spatial electromagnetic wave signals are captured by an array antenna; these signals are then amplified, undergo phase compensation, and receive amplitude compensation via a receiving channel; subsequently, multiple-channel signals are synthesized using a power divider and a combiner to form a spatial beam, an azimuthal beam, and a pitch-angle beam, which are then transmitted to the backend receiver. During transmission, the RF excitation signal passes through the power divider and combiner, is divided into multiple transmission channels, undergoes phase compensation and amplification via the TR module's transmission channel, and is ultimately output to the antenna to generate a beam in a specified spatial direction.

Product function

a） State information such as the temperature and current of each sub-array can be reported in real time via wave control;

b） The PWM controller regulates the fan speed.

Product Coordinate System Definition



说明：
OP：为波束指向
b：方位角，为波束指向OP在XOZ面的投影OJ与OM的夹角∠JOM
a：俯仰角，为波束指向OP在XOZ面的投影OJ与OP的夹角∠JOP
θ：离轴角，为波束指向OP与OM的夹角∠MOP
φ：旋转角，为波束指向OP在YOZ面投影OH与OL的夹角∠LOH

Figure 1: Definition of the phased array antenna coordinate system

2.Qualification

Platform Performance Specifications

The product technical specifications are shown in the table below; all specified parameters refer to conditions at room temperature.

NO.	name of index	Indicator Requirements
1.	Operating frequency band	9.2GHz ~ 9.8GHz
2.	Operating frequency	The frequency step typical value is 30 MHz; it can be customized according to user requirements.
3.	Antenna Type	Active 2D scanning phased array antenna; azimuth–elevation 2D scanning
4.	Polarization method	Typical configuration: Vertical polarization (Notes: horizontal polarization modification can be performed as

NO.	name of index	Indicator Requirements
		required.)
5.	Array Size	Cross-shaped, 1024 minus 4 corners (8×8 grid cells) Total number of units: N = 1024 – 8 × 8 × 4 = 768
6.	Antenna Gain (Normal Direction)	Output: ≥33.2 dB (unweighted, as specified in the design) Reception: ≥32.2 dB (weighted, design guarantee)
7.	EIRP (Normal)	≥89.5 dBm @ full frequency band, across all temperatures
8.	G/T (Normal)	≥5 dB/°K across all frequency bands and over all temperature ranges
9.	Electrostatic scanning range	Azimuth ±45°, Pitch ±40°
10.	beam-pointing accuracy	Pointing error ≤ 0.3°; (within ±45° scan range) Pointing error ≤ 0.15°; (within ±20° scan range)
11.	Scan Down	Azimuth direction: ≤3 dB (within ±45° scan range) Pitch/roll: ≤3 dB (within ±40° scan range)
12.	Transmitter azimuth plane normal beam width	3.4° ± 0.3° @ center frequency point
13.	Transmitter pitch-plane normal beam width	3.4° ± 0.3° @ center frequency point
14.	Receiver azimuth normal beam width	3.8° ± 0.4° @ center frequency
15.	Received pitch-plane normal beam width	3.8° ± 0.4° @ center frequency

NO.	name of index	Indicator Requirements
16.	Received azimuth-based normal component of the first sidelobe level (normal direction)	≤-22dB
17.	Receive the first sidelobe level (normal direction) of the pitch plane	≤-22dB
18.	Receiving method for the zero-depth (normal) normal difference beam	Directional gain: -22 dB (typical value) Pitch: -22 dB (typical value)
19.	Reception channel active gain	≥15 dB (Design guarantee; adjustable)
20.	Receiver channel noise figure	<3.5 dB across all frequency bands and operating temperatures (as specified in the design);
21.	Duty cycle	Up to 20%
22.	Transmitter excitation power	30±2dBm
23.	weighting scheme	Receives default weighting; transmits without weighting.
24.	Product Power Consumption	≤800W (emission duty cycle: 20%)
25.	Beam handover time	≤70us

3.Weight ≤14Kg

4.Product appearance and dimensions

Product external dimensions

≤630 mm (azimuth) × 630 mm (pitch) × 65 mm (thickness).

Appearance and Surface Condition

Conductive oxide coating for the metal cavity surface (natural or colored); white primer spraying applied to the antenna housing surface.

Product Structure Exterior View Diagram

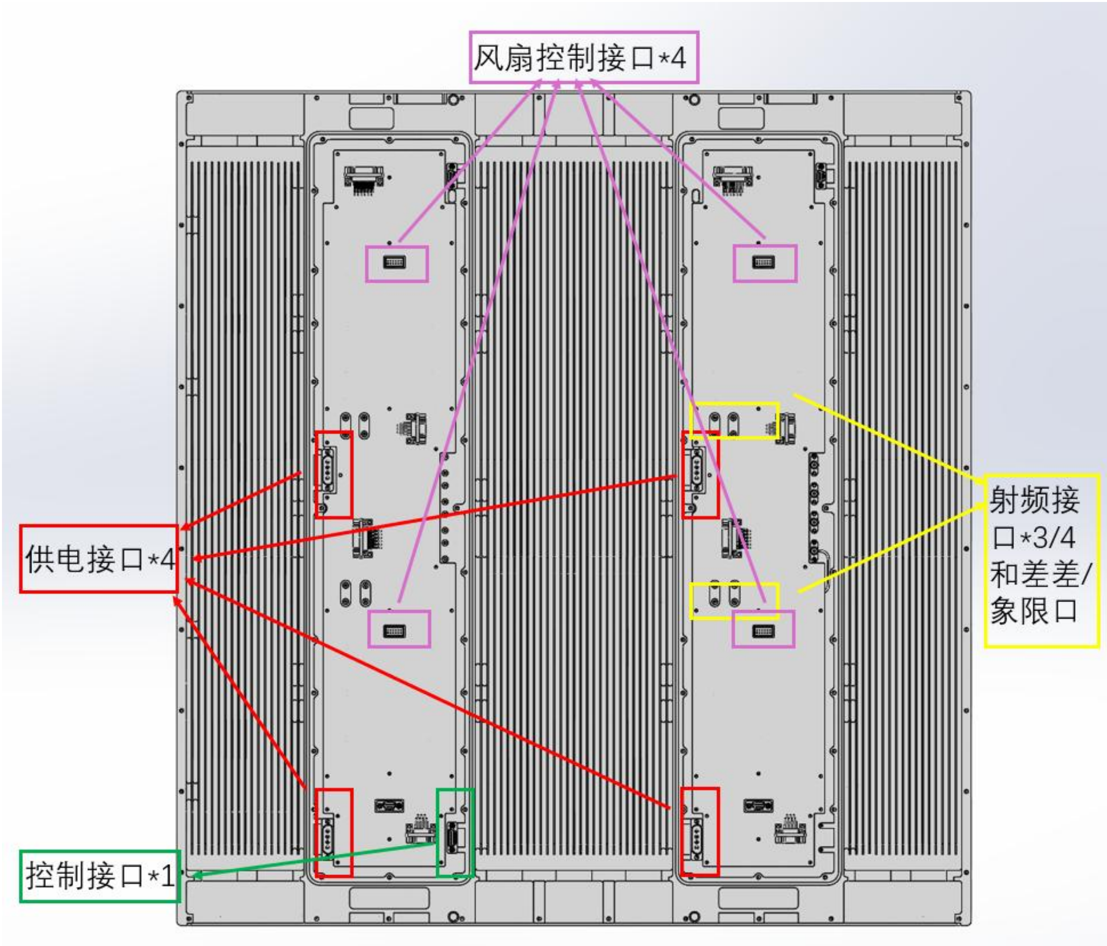


Figure 1: Overall structural schematic diagram

The entire device features 4 power supply interfaces, 1 control interface, 4 fan control interfaces, and 1 RF interface. The RF interface supports 3 analog differential I/O channels and 4 quadrant I/O channels.

The default fan control interface for 4 fan groups uses PHB2.0 connectors; this configuration does not include power supply functionality, but supports custom J30J-9ZK fan power supply control connectors, allowing the fans to be installed in locations as close as possible to their intended positions.

5.Product power supply requirements

Main power input voltage: DC 18V–36V

6.Interface Requirements

The RF interface uses SMA-K; the interface definition is shown in the table below (default configuration includes analog and differential signals):

Table 1: RF Interface Table

NO.	name	definition	direction	remarks
1	H	Phased-Array RF Input/Output 1	Phased Array <-> Frequency Synthesizer	Receive and transmit excitation ports
2	FWC	Phased-array RF Output 2	Phased array → Frequency synthesizer	Receiver azimuth difference
3	FYC	Phased-array RF Output 3	Phased array → Frequency synthesizer	Receive pitch difference

The control interface uses J30J-15ZK; the interface definition is shown in the table below.

Table 1: Control Interface Table

Pin number	Signal Name	Signal Definition	Signal Direction	explain
1	RXD+	Serial port receive data differential positive terminal	Data Acquisition Board-> Phased Array	RS422
2	RXD-	Serial port receive data differential negative terminal	Data Acquisition Board-> Phased Array	RS422
3	TXD+	Serial port data differential positive terminal	Phased Array → Data Acquisition Board	RS422
4	TXD-	Serial port data differential negative terminal	Phased Array → Data Acquisition Board	RS422
5	CLK+	Serial port receive clock differential positive terminal	Data Acquisition Board-> Phased Array	RS422(10MHz)
6	CLK-	Serial port receive clock differential negative terminal	Data Acquisition Board-> Phased Array	RS422(10MHz)
7	TRT+	Positive terminal of the transmit/receive switching signal	Data Acquisition Board-> Phased Array	RS422
8	TRT-	Negative terminal of the transmit-receive switching signal	Data Acquisition Board-> Phased Array	RS422

9	LD+	Feed the amplitude-phase data into the positive terminal of the signal.	Data Acquisition Board-> Phased Array	RS422
10	LD-	Feed the amplitude-phase data to the negative terminal of the signal.	Data Acquisition Board-> Phased Array	RS422
11	GND_COM	the earth	Data Acquisition Board <-> Phased Array	Signal Ground
12	TRR+	Positive terminal of the transmit/receive switching signal	Data Acquisition Board-> Phased Array	RS422
13	TRR-	Negative terminal of the transmit-receive switching signal	Data Acquisition Board-> Phased Array	RS422
14	BF+	reserve	Data Acquisition Board-> Phased Array	RS422
15	BF-	reserve	Data Acquisition Board-> Phased Array	RS422

The power supply interfaces use the J30J04P040 type, with a total of 4 sets; each set has identical interface definitions.

Table 1: Power Supply Interface Definitions

order number	Jumper cable numbering	Signal Definition
1	A	+24V
2	B	+24V
3	C	GND
3	D	GND

The fan power supply control connector is customizable to support J30J-9ZK; each interface set has consistent definitions.

Table 1: Fan Power Supply Control Connector

Pin number	Signal Name	Signal Definition	Signal Direction	explain	remarks
1	VCC	Fan-powered supply	Phased array-> Fan	+12V power supply (or consistent with the overall system input)	The fan feedback pin should be wired
2	GND	GND	Phased	GND	

			array-> Fan		separately; the speed control pin and the power supply pin can be combined into a single input line.
3	FS_FG1	Fan Feedback	Fan → Phased Array	Fan 1 Feedback	
4	FS_FG3	Fan Feedback	Fan → Phased Array	Fan 3 Feedback	
5	FS_PWM	Fan speed control	Phased array-> Fan	Fan speed control pin	
6	VCC	Fan-powered supply	Phased array-> Fan	+12V power supply (or consistent with the overall system input)	
7	GND	GND	Phased array-> Fan	GND	
8	FS_FG2	Fan Feedback	Fan → Phased Array	Fan 2 Feedback	
9	FS_FG4	Fan Feedback	Fan → Phased Array	Fan 4 Feedback	

7.environmental suitability

a)Operating temperature: -40°C to +60°C;

b)Storage temperature: -50°C to +70°C.

8.other

Meets general environmental requirements for electromagnetic compatibility, vibration, rain exposure, wind resistance, and other basic conditions.

9.Communication Protocol Requirements

The detailed communication protocol is tentatively specified in Appendix I; it may be customized or modified upon negotiation.

Annex 1: X-band Two-Dimensional Phased Array Antenna Communication Protocol

The parameter transmission between the Signal Processing Board and the Wave Control Board is achieved via a synchronous RS422 interface. CLK± provides the communication clock signal (≥10 MHz) from the Signal Processing Board to the Wave Control Board; RXD± represents the signal used by the Signal Processing Board to transmit data to the Wave Control Board; TXD± represents the signal used by the Wave Control Board to transmit data to the Signal Processing Board; and LD± serves as the control signal that, after the Signal Processing Board transmits parameters to the Wave Control Board, controls the binding parameters of the Wave Control Board to the Multi-function Chip.

When transmitting data packets via a synchronous serial interface, the transmitter updates the data at the rising edge of the clock signal and transmits the data at the falling edge. The transmitter first sends a 1-bit start bit (low-level active), followed by the data payload of the packet; the transmission order is such that packets with smaller sequence numbers are transmitted before those with larger sequence numbers. For single-byte transmissions, the higher-order bits of the byte are sent first, followed by the lower-order bits. If the packet content consists of multiple bytes, it is transmitted according to the big-endian mode (i.e., the high-order byte is sent first, followed by the low-order byte). Once all data packets have been transmitted, the transmitter sets the corresponding data signal lines to a high level, entering an idle state.

After the Wave Control Board sends a control command to the Signal Processing Board, it simultaneously sends a set of packet data back to the Signal Processing Board as a command response; except for the packet type, which may differ from the Signal Processing Board's command, the remaining content of this response packet shall be consistent with the Signal Processing Board's command. Upon receiving the status information command packet, the Wave Control Board sends a status information packet back to the Signal Processing Board.

The control command message sent from the signal board to the wave control board is as follows:

Table 1: Data acquisition transmission wave control information packet (16 bytes)

order number	Signal Name	Number of bytes	explain	remarks
1	heading	1	0xAA	----
2	Message Type	1	0x13	Wave Control Response Data
3	Message length	1	0x10	The packet length is 16 bytes.

order number	Signal Name	Number of bytes	explain	remarks
4	control word	1	0x80	Bit7–Bit6: Default is 2b10
	frequency code			Bit5–Bit0 frequency encoding: 1–9.2 GHz, 2–9.23 GHz,..., 21–9.8 GHz
5	work pattern	1	0x01	Transmit/Receive Control: 00: Reserved; 01: Receive Mode 10: Transmitter operation; 11: Transmitter and receiver operate simultaneously
6~7	Azimuth angle encoding	2	0x0000	Unsigned integer formatting; quantization unit: 0.05°; valid range: 0–2000.0: –50.00°; 1: –49.95°; 2: –49.90°; 2000:50°
8~9	Pitch angle encoding	2	0x0000	Unsigned integer conversion; quantization unit: 0.05°; valid range: 0–2000; 0: –50.00°; 1: –49.95°; 2: –49.90°; 2000:50°
10~11	channel switch	2	0xffff	Unsigned integer formatting; 1,024 channel selection options: 0: All channels disabled; 1: Channel 1 enabled; 2: Channel 2 enabled; 1024: Channel 1024 enabled; 0xFFFF: All channels enabled
12	Phase Enable	1	0x01	Default value: 1
13	Attenuation Enable	1	0x01	Default value: 1
14-16	Reserve	3	0x0000000	Default value: 0

Table 1: Wave Control Send Response Command Message (16 bytes)

order number	Signal Name	Number of bytes	explain	remarks
1	heading	1	0xAA	----
2	Message Type	1	0x13	Wave Control Response Data
3	Message length	1	0x10	The packet length is 16 bytes.
4	control word	1	0x80	Bit7–Bit6: Default is 2b10
	frequency code			Bit5–Bit0 frequency encoding: 1–9.2 GHz, 1–9.23 GHz,..., 21–9.8 GHz
5	work pattern	1	0x01	Transmit/Receive Control: 00: Reserved; 01: Receive Mode 10: Transmitter operation; 11: Transmitter and receiver operate simultaneously
6~7	Azimuth	2	0x0000	Unsigned integer formatting;

	angle encoding			quantization unit: 0.05°; valid range: 0–2000.0: –50.00°; 1: –49.95°; 2: –49.90°; 2000:50°
8~9	Pitch angle encoding	2	0x0000	Unsigned integer conversion; quantization unit: 0.05°; valid range: 0–2000; 0: –50.00°; 1: –49.95°; 2: –49.90°; 2000:50°
10~11	channel switch	2	0xffff	Unsigned integer formatting; 1,024 channel selection options: 0: All channels disabled; 1: Channel 1 enabled; 2: Channel 2 enabled; 1024: Channel 1024 enabled; 0xFFFF: All channels enabled
12	Phase Enable	1	0x01	Default value: 1
13	Attenuation Enable	1	0x01	Default value: 1
14-16	Reserve	3	0x0000000	Default value: 0

Table 1: Wave Control Transmission of Monitoring Command Information Packet (36 bytes)

NO.	**Signal Name**	**Number of bytes**	**explain**	**remarks**
1	heading	1	0xAA	----
2	Message Type	1	0x32	PWM control status information
3	Message length	1	0x24	The packet length is 36 bytes.
4~19	Temperature information	16		Every two bytes represent one channel array.
20~35	Current Information	16		Every two bytes represent one channel array.
36	Fan Information	1		Every two representatives correspond to one fan (01 indicates normal operation).

The control timing sequence between the Signal Processing Board and the Wave Control Board primarily consists of two components: the communication control timing sequence and the transmit-receive switching control timing sequence. The figure below illustrates the control command transmission from the Signal Processing Board to the Wave Control Board, the reception of wave control status information, and the transmit-receive control timing sequence. Each data packet contains only one start bit and one stop bit; thus, a 16-byte data packet corresponds to a packet length of 16 × 8 bits + 2 bits (start bit/stop bit) = 130 bits.

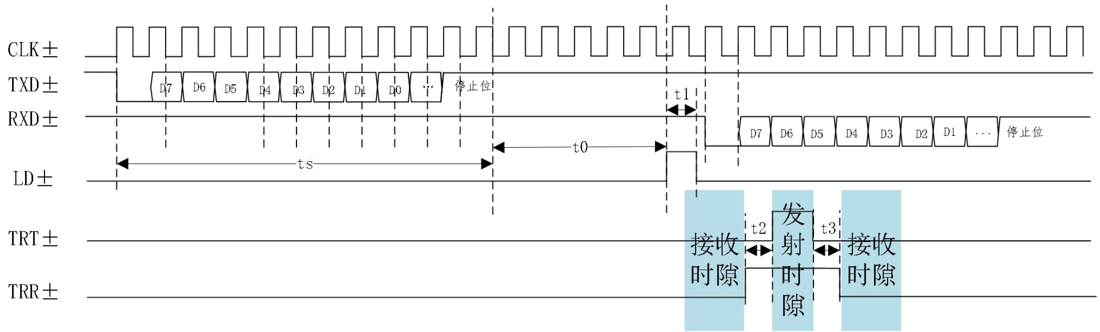


Figure 1: Data write and transmit/receive wave control timing diagram

Monitoring command sequence description: Bytes 4–19 contain two-byte temperature data for each channel (TEMP_CHANL1, TEMP_CHANL2, TEMP_CHANL3, TEMP_CHANL4, TEMP_CHANL5, TEMP_CHANL6, TEMP_CHANL7, TEMP_CHANL8). The temperature conversion formula is: TEMP × 0.625 / 10.

The current information for each channel (2 bytes per channel), in order from 20 to 35, is: (CURRENT_CHANL1, CURRENT_CHANL2, CURRENT_CHANL3, CURRENT_CHANL4, CURRENT_CHANL5, CURRENT_CHANL6, CURRENT_CHANL7, CURRENT_CHANL8).

Current conversion formula:

$$\text{Current} = \underline{D[14{:}0]} \bullet 19.42\mu V/R_{SENSE}, \text{ if Sign} = 0$$

Here, Rsense = 0.01. The 36 bytes contain fan information: every two bytes represent one fan; '01' indicates normal operation; for example, '01010101' represents four fans operating normally.